

Please cancel claims 1-8 and 50.

Please add new claims 51-62 as follows:

Sub D1

51. (New) An integrated circuit comprising:  
a semiconductive substrate;  
a diffusion region formed within the substrate, the diffusion region and substrate forming a junction;  
a conductive line formed over the substrate and diffusion region, the conductive line having a generally uniform lateral width, and a portion of the conductive line over the diffusion region comprising an entirety of the lateral width of the conductive line received directly over the diffusion region; and  
wherein the junction is configured to be reverse biased to preclude electrical shorting between the conductive line and the substrate for selected magnitudes of current provided through the conductive line.

C1

52. (New) The integrated circuit of claim 51 wherein the diffusion region comprises a portion disposed outwardly from directly beneath the conductive line.

53. (New) The integrated circuit of claim 51 wherein the diffusion region comprises two portions disposed outwardly from directly beneath the conductive line.

54. (New) The integrated circuit of claim 51 wherein the diffusion region comprises two portions disposed outwardly from directly beneath the conductive line, a first portion outward of a first side of the conductive line and a second portion outward of a second side of the conductive line.

55. (New) An integrated circuit comprising:

a semiconductive substrate;

a diffusion region formed within the substrate, the diffusion region and substrate forming a junction;

a conductive line formed over the substrate and the diffusion region;

a conductive material interconnecting the conductive line and the diffusion region, an entirety of the conductive material received directly over the diffusion region; and

wherein the diffusion region is configured to be reverse biased to preclude electrical shorting between the conductive line and the substrate through the conductive material for selected magnitudes of current provided through the conductive line.

56. (New) The integrated circuit of claim 55 wherein the diffusion region comprises a portion disposed outwardly from directly beneath the conductive material.

57. (New) The integrated circuit of claim 55 wherein the diffusion region comprises at least two portions disposed outwardly from directly beneath the conductive material.

58. (New) The integrated circuit of claim 55 wherein the conductive material comprises metal.

59. (New) An integrated circuit comprising:

- a semiconductive substrate;
- a diffusion region formed within the substrate, the diffusion region and substrate forming a junction;
- a conductive line formed over the substrate and the diffusion region;
- a conductive material interconnecting the conductive line and the diffusion region, a portion of the conductive material received directly over the conductive line, and an entirety of the portion of the conductive material received directly over the diffusion region; and

wherein the diffusion region is configured to be reverse biased to preclude electrical shorting between the conductive line and the substrate through the conductive material for selected magnitudes of current provided through the conductive line.

60. (New) The integrated circuit of claim 59 wherein the diffusion region comprises a portion disposed outwardly from directly beneath the combined cross-sectional area of the conductive material and the conductive line.

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61. (New) The integrated circuit of claim 59 wherein the diffusion region comprises at least two portions disposed outwardly from directly beneath the combined cross-sectional area of the conductive material and the conductive line.

*Sub 02.*  
62. (New) The integrated circuit of claim 59 wherein the conductive material comprises metal.

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